Simulation of Single Electron Transistor Inverter Neuron: Memory Application

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Abstract

With respect to single-electron transistor (SET) technology, it is possible to build neural networks with extreme low power properties. To simulate SET circuits, an electrical model has been represented. In contrast to the prescriptions in the so-called Orthodox theory of single-electronics, this model explores the discrete character of the tunnel current and conditions.

In this paper a brief description of neural circuitry based tree-island structure was given and verified as a single-electron memory SEM with a well known SET device simulator called SIMON.

Keywords

Single Electron Transistor; Single Electron Memory; Neural network; Orthodox Theory; MATLAB; SIMON

Introduction

One of the most promising new devices based on new nanoscale physics is the single-electron transistor "SET". A SET has an extremely small quantum dot in the channel. The number of electrons in the dot is precisely controlled by the Coulomb blockade, and a SET shows unique oscillatory I-V characteristics that are expected to have new functionalities. A great deal of research has been done on the realization of memory devices based on the single electron tunneling phenomena. A single electron memory "SEM" should work with a reasonable bit error rate which has low power, scalability to the sub-nanometer regime and extremely high charge sensitivity.Several other applications of analog single-electron devices in unique scientific instrumentation and metrology seem quite feasible because the prospect of silicon transistors being replaced by single-electron devices in integrated digital circuits, faces tough challenges and remains uncertain.

On the other hand, artificial neural networks "ANNs" seem to be surrounded by a great deal of mystique and, sometimes, misunderstanding. Neural networks are often supposed to have brain behavior qualities, problem-solving abilities, learning capacity and self-awareness. Neural Networks offer improved performance over conventional technologies in areas which include: Machine Vision, Robust Pattern Detection, Signal Filtering, Virtual Reality, Data, Complex Mapping and more.

In this paper, we present simulations of typical SET I–V characteristics using MATLAB. The main point of our work consists in the proposition of a neural circuitry based on single electron transistor as a model of a SET/SEM device. In order to have an idea about capacitances and resistances of tunnel junction, we present SEM simulation obtained results with SIMON.

The Single Electron Device

The Orthodox Theory

Throughout the history of single electronics, a few theories have been proposed to form the basis of a theory for circuits including single electron tunneling devices. The most widely applied one is the orthodox theory of single electronics. This theory was developed by Averin and Likharev. It is a model describing the basic physics of single-electron devices based on the free (electrostatic) energy of the system under consideration. In the orthodox theory, an adequate measure of the strength of this effect is the charging energy$E_c = \frac{e^2}{C_{tot}}$, where C_{tot} is the total capacitance. In fact, the orthodox theory makes the following five major assumptions:

- Random background charges and initial charges on the islands are neglected.
- Cotunneling is ignored.

- Tunneling time is negligibly small in comparison with other time scales like time interval between two successive events.

These assumptions simplify the equations, but do not limit the description. The electron tunneling through a junction is always a random event with a certain rate Γ (probability per unit time), which is related to free electrostatic energy ΔF of the system. This energy depends on the tunnel resistance R_{tot}, and the temperature T.

The Single Electron Transistor

The functioning of the SET is based on the Coulomb blockade theory, which is a direct consequence of the discreteness of the electron charge. In order to develop the I-V characteristic, we start by analyzing the equivalent electrical model of SET Fig .1 using Kirchhoff voltage and current laws.

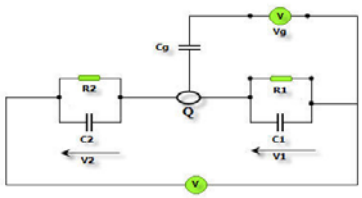

FIG.1 SINGLE ELECTRON TRANSISTOR EQUIVALENT CIRCUIT

The electrical model of the single electron transistor is composed of an island between two tunnel junctions, which is modeled with a resistance parallel with capacitor and related to a gate voltage by a capacitor. The gate which is biased with a voltage V_G creates a charge in the island:

$$Q_G = C_G(V_G - V_1) \tag{1}$$

Where the potentials V_1 and V_2 are as a function of Q

$$\begin{cases} V_1 = \dfrac{Q + C_2 V}{C_1 + C_2} \\ V_2 = \dfrac{-Q + C_1 V}{C_1 + C_2} \end{cases} \tag{2}$$

As a consequence of a tunnel event, the number N of electron in the island change and there is a variation of the system total energy ΔE *Eq.3*

$$\begin{cases} \Delta E_1^{\pm}(V) = \dfrac{(Q \pm q)^2}{2C_{tot}} - \dfrac{Q^2}{2C_{tot}} \pm q\dfrac{C_2}{C_{tot}}V \\ \Delta E_2^{\pm}(V) = \dfrac{(Q \pm q)^2}{2C_{tot}} - \dfrac{Q^2}{2C_{tot}} \pm q\dfrac{C_1}{C_{tot}}V \end{cases} \tag{3}$$

(+ and - correspond to the electron transfer from the high and low potential consequently)

The rate Γ of tunneling events is given by the orthodox theory:

$$\Gamma_j^{\pm}(R_j, \Delta E_j^{\pm}) = \frac{1}{R_j q^2}\left(\frac{-\Delta E_j^{\pm}}{1 - \exp\left(\frac{\Delta E_j^{\pm}}{kT}\right)}\right) \tag{4}$$

Rj is the resistance the *jth* tunnel junction.

Using *Eq.4*, the probability to have N electrons in the island is calculated with Master Equation:

$$\begin{aligned} \frac{dP(N,V)}{dt} &= P(N-1,V)\left\{\Gamma_1^+(N-1,V) + \Gamma_2^-(N-1,V)\right\} \\ &+ P(N+1,V)\left\{\Gamma_1^-(N+1,V) + \Gamma_2^+(N+1,V)\right\} \\ &- P(N,V)\left\{\Gamma_1^+(N,V) + \Gamma_1^-(N,V) + \Gamma_2^+(N,V) + \Gamma_2^-(N,V)\right\} \end{aligned} \tag{5}$$

Then the probability expression after normalizing is:

$$\begin{cases} \left(\sum_{i=N_0-\Delta N}^{N_0+\Delta N} P(i,V)\right)^{-1} & N = N_0 \\ \dfrac{\prod_{i=N_0}^{N+1} Y(N,V)}{\prod_{i=N_0-1}^{N} X(N,V)}\left(\sum_{i=N_0-\Delta N}^{N_0+\Delta N} P(i,V)\right)^{-1} & N_0 - \Delta N \le N < N_0 \\ \dfrac{\prod_{i=N_0}^{N-1} X(N,V)}{\prod_{i=N_0+1}^{N} Y(N,V)}\left(\sum_{i=N_0-\Delta N}^{N_0+\Delta N} P(i,V)\right)^{-1} & N_0 < N \le N_0 + \Delta N \\ 0 & N < N_0 - \Delta N \quad N > N_0 + \Delta N \end{cases} \tag{6}$$

N_0 is the number of electrons corresponding to the most stable state.

Current versus voltage can be calculated on any junction according to the following equation:

$$\begin{aligned} I_1(V) &= q\sum_{i=N_0+\Delta N}^{N_0+\Delta N} P(i,V)\left[\Gamma_1^+(i,V) - \Gamma_1^-(i,V)\right] \\ I_2(V) &= q\sum_{i=N_0+\Delta N}^{N_0+\Delta N} P(i,V)\left[\Gamma_2^+(i,V) - \Gamma_2^-(i,V)\right] \end{aligned} \tag{7}$$

1) Transfer Function

The transfer function of a SET is the relationship between an input signal at the gate and the output signal at the drain of the device. The output can be either a voltage or a current, depending on whether the transistor is current or voltage biased.

The current biased SET transistor has a periodic transfer function; this is explained with the aid of fig .2 which shows V_{ds} and the junction voltages V_{di} and V_{is}.

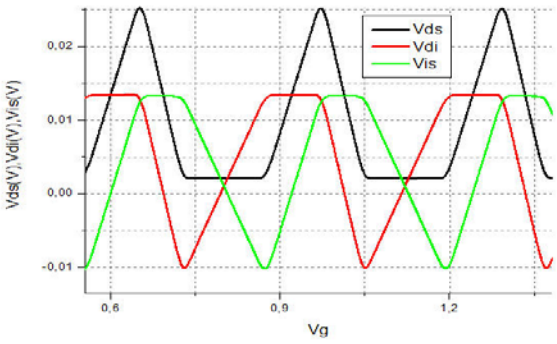

FIG.2.DRAIN-SOURCE VOLTAGE AND JUNCTION VOLTAGES AS A FUNCTION OF THE GATE VOLTAGE FOR A CURRENT BIASED SET TRANSISTOR

We see that for the positive slope of V_{ds} the voltage across the source junction is constant at the edge of coulomb blockade for that junction. In this part of the curve electrons first tunnel through the source junction and then through the drain junction. With increasing V_g, the voltage across the drain junction steadily increases to the coulomb blockade level. At this point, there is no preference for tunneling first through the drain or the source.

As V_g increases further, the voltage which is only possible if the source junction voltage decreases rapidly to counteract the effect of the gate voltage. When V_{ds} is at its minimum, an additional electron is transferred to the island, which restores the original voltage situation.

Single Electron Memories

Various designs have been proposed during the past years to establish a better overview of the state of the single electron memories art such as the single electron flip-flop, the ring memory, Q_0-Independent Memory, electron-trap and others which have a different functionality.

The power consumption of SET memories is usually smaller than that of conventional memories, due to the minuteness of capacitances and the limited number of electrons concerned in charging and discharging.

One of the most promising applications of single electronics is the single-electron memory fig.2. To have a good single electron memory operation, some criteria are necessary. The First criterion is the operation temperature. In fact, the memory cell must be operated at room temperature. Secondly, its bits error rate must be reasonable, along with low power consumption. Manufacturability is the last but not the least criterion.

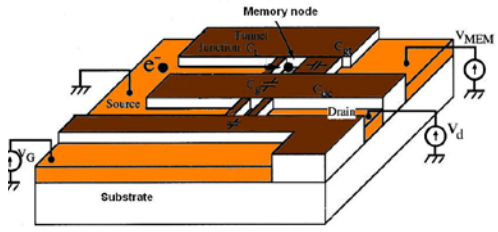

FIG.2 DESIGN OF "SEM" WHICH IS FORMED OF TWO BLOCS: THE MEMORY BLOC (WRITE/ERASE PROCESS) AND READING BLOC

Neural Network

The Neural Biological Model

Neurons are basic signaling units of the nervous system of a living organism in which each neuron is a discrete cell whose several processes are derived from its cell body.

The human brain contains more than a billion of neuron cells, and each cell works like a simple processor. The massive interaction between all cells and their parallel processing only makes the brain's abilities possible.

The biological neuron has four main regions to its structure fig.3: The cell body or soma, the dendrites, the axon and synapses.

The cell body is the heart of the cell. It contains the nucleolus and maintains protein synthesis. Dendrites which receive signals from other neurons, a single neuron usually has one axon, whose main function is to conduct electrical signals generated at the axon hillock down its length.

These signals are called action potentials. The other end of the axon may split into several branches, which end in a pre-synaptic terminal. The electrical signals what the neurons use to convey the information of the brain are all identical.

The brain analyzes all patterns of sent signals, and from that information it interprets the type of received information. The synapse is the area of contact between two neurons. They do not physically touch because they are separated by a cleft. The electric signals are sent through chemical interaction. The neuron sending the signal is called pre-synaptic cell and the neuron receiving the electrical signal is called postsynaptic cell.

The electrical signals are generated by the membrane potential which is based on differences in

concentration of sodium and potassium ions and outside the cell membrane.

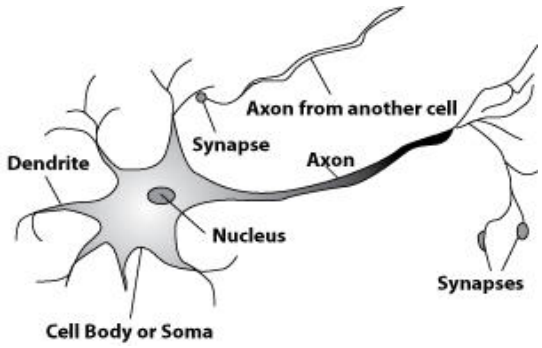

FIG.3 BIOLOGICAL NEURON MODEL

Artificial Neural and Mathematical Model

The artificial neuron is a processor unit composed of four functional elements as we can see in Fig.4

- The receptor is the block where the inputs x_i arrives. These inputs are signals coming from the environment or from other neurons that are attenuated or amplified by a weighting factor. These weights are adapted to the specific problem through a learning algorithm.
- The adder, that implements the weighted sum of the inputs, according to following expression:

$$S = \sum_{i=1}^{n} w_i x_i \qquad (8)$$

- The activation function, that applies a non-linear threshold function to the adder output to decide if the neuron fires or not. This function is usually a sigmoid function.
- The output element that produces and distributes the corresponding output.

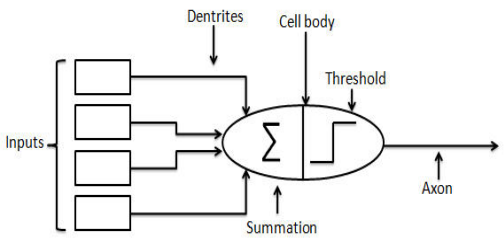

FIGURE 4 ARTIFICIAL NEURON MODEL

SET Neural Circuits:

The ultimate goal of building neural networks with a single-electron transistor is to make large neural networks with high processing power. For this reason various research groups suggested neural network nodes based on SET circuit primitives and SET devices.

The first circuit ideas date from the end of 1995 (C_SET based) Central in the design is the C-SET transistor in series with a current source**.** Gerousis et al suggested a node for a cellular neural network based on a three-island structure.

Fig.5 shows the neural circuitry 3-island based where C_{c1}, C_{c2} the addition capacitors, C_{c3}, C_{c4} the coupling capacitors, V_{in1}, V_{in2}, V_{in3}…..V_{inN} are the inputs voltages and V_{out} is the output voltage

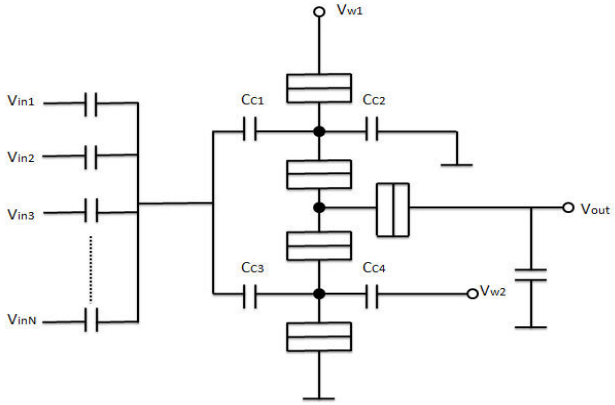

FIG.5. PROPOSED SET-BASED NEURAL CIRCUITRY 3-ISLAND BASED

The weight is represented as a voltage at the drain of the three islands structure. This neural is composed of a multiplication, an adding and an activation function. The adder is obtained by capacitive coupling, the activation function by cascading two C-SET transistors and the weight is represented as a voltage at the drain of the 3 islands. The circuit receives a voltage input from a sum-of-product unit to generate its internal state and produces the corresponding voltage output.

Results and Simulation:

MATLAB Simulation

In this section, we present *I–V* characteristics using the orthodox theory. A flow diagram represents the algorithm used in MATLAB is shown in fig.6

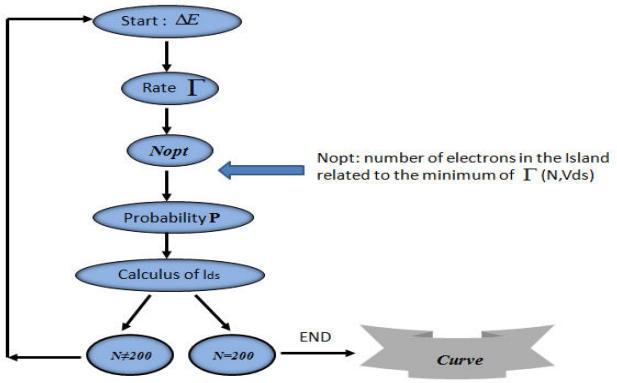

FIG. 6 FLOW DIAGRAM USED IN MATLAB

In MATLAB code, after we have taken some initialization, we have calculated the total energy variation and the rate for different configurations. In order to obtain N_{opt} there are many methods, and we have chosen the lientschnig method where

$$N_{opt} = \frac{C_g \times V_g \times (R_r + R_l) - R_r \times (C_r + C_g) \times V_{ds} + C_l \times R_l \times V_{ds}}{e \times (R_r + R_l)} \quad (8)$$

Then we can calculate the different transition probabilities to finally get I-V characteristic using Eq.7

1) I_{ds} –V_{ds} characteristics:

Using the orthodox theory in MATLAB simulator, we get the corresponding Fig. 7 and fig. 8.

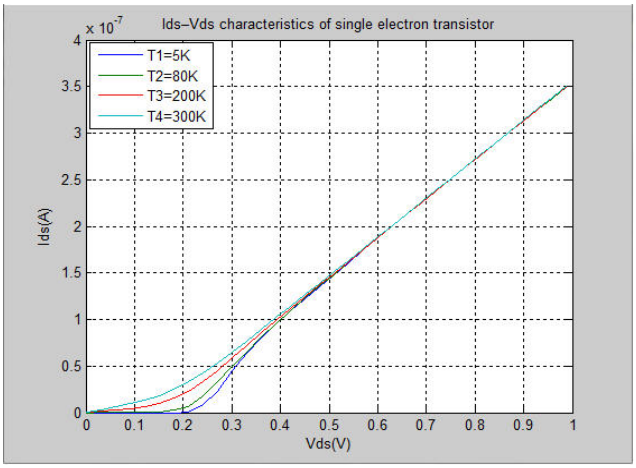

FIG.7 THE CURRENT – DRAIN VOLTAGE CHARACTERISTICS FOR DIFFERENT TEMPERATURES WITH THE PARAMETER VALUES ARE C_1=0.15 AF, C_2= 1.5 AF, C_G= 0.4 AF, R_1=1.91 MΩ, R_2= 0.38 MΩ AND THE DRAIN VOLTAGE IS 0.9 V

The effects of temperature on I_{ds}-V_{ds} characteristics of SET are demonstrated in fig.7 and it shows that the Coulomb blockade region becomes thinner at higher temperature for example (300K). This is because of the influence of thermal energy, which is in the same order of the biased drain-source voltage and which affects the state of the dot charge.

Fig.8 represents the current drain voltage characteristics for different bias V_g, which illustrates the blockade effect. The effect prevents current from flowing until it exceeds a certain voltage, at which point the blockade breaks down. The breakdown voltage depends on gate charge that is why the curves are different. Comparing the I_{ds}-V_{ds} characteristic we notice that the current suppression region increases, respectively, from V_{gs}=0.1V to 0.9V

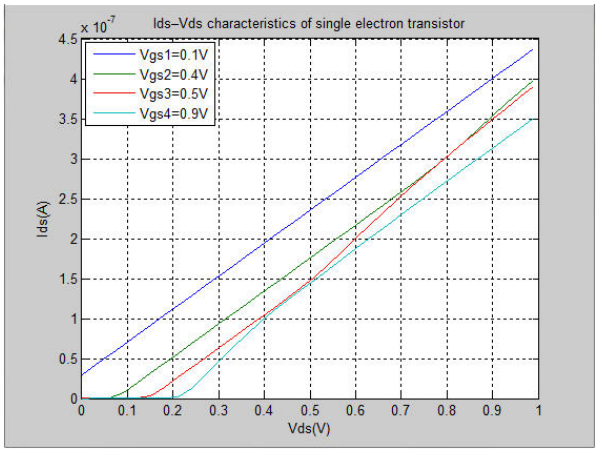

FIG.8 THE CURRENT – DRAIN VOLTAGE CHARACTERISTICS FOR DIFFERENT BIAS WITH THE PARAMETER VALUES ARE C_1=0.15 AF, C_2= 1.5 AF, C_G= 0.4 F, R_1=1.91 MΩ, R_2= 0.38 MΩ AND T=50K

2) Ids –Vgs Characteristics:

In Fig.9 and Fig.10, we clearly illustrate Coulomb Oscillations. The oscillations are the drain currents versus the gate input voltages.

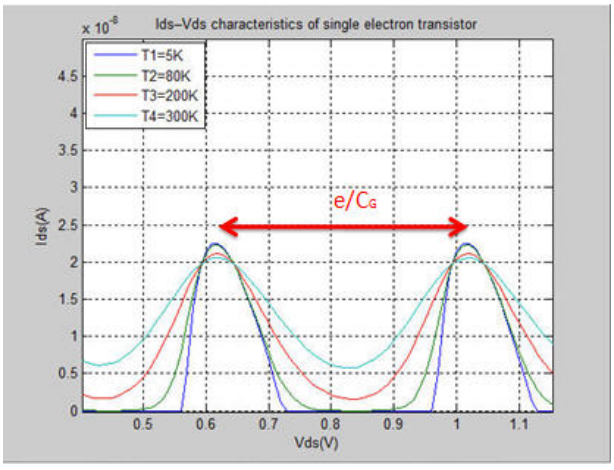

FIG.9 THE DRAIN CURRENT AS FUNCTION OF GATE VOLTAGE CHARACTERISTICS FOR DIFFERENT TEMPERATURE WITH THE PARAMETER VALUES ARE C_1=0.15 AF, C_2= 1.5 AF, C_G= 0.4 AF, R_1= 1.91 MΩ, R_2=0.38 MΩ AND THE DRAIN VOLTAGE IS 9 MV

We need to know the shape of the oscillation curves in order to bias the SETs for correct logical operation. Otherwise, we could wind up with a situation such as

the SET conducting current for both logic 1 and logic 0 inputs.

Fig.9 displays the temperature dependence of the peaks in the classical regime. At low temperatures, there are sharp Coulomb blockade peaks because the number of electrons in a dot in the valleys is almost quantized. At higher temperatures, electrons can be excited on and off the central island at values of gate voltage in close proximity to these points, forming a large peak. It also shows that the SET Coulomb blockade oscillation period ($\frac{e}{CG}$, e is the electronic charge) is dictated by SET gate capacitance.

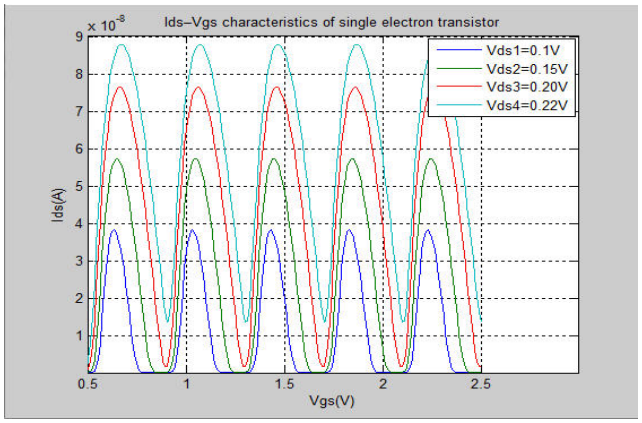

FIG.10 THE CURRENT DRAIN VERSUS GATE VOLTAGE CHARACTERISTICS FOR DIFFERENT BIAS WITH THE PARAMETER VALUES ARE C_1=0.15 AF, C_2= 0.15 AF, C_G= 0.4 AF, R_1= 1.91 MΩ, R_2=0.38 MΩ AND T=50K

The effects of V_{ds} on Coulomb oscillations are demonstrated in Fig.10. The irregularity of oscillations and their different peak heights can be explained by fluctuations of the polarization charge. The flat portion of this curve signifies that a finite V_{ds} is needed to overcome the Coulomb barrier. The width of this flat portion is periodically modulated by the gate voltage. The source-drain voltage bias that corresponds to the maximum SET response is V_{ds}=0.1V.

SIMON Simulations

In this section, we are going to take electric schema of the neuron based on SET described in the previews section and try to investigate the relation between the device's geometric parameters and the single-charging effects in the electrical characteristics. A simplified electrical model is shown in the following figure (Fig.11)

The shape of control signals (the inputs) is very important to observe the charge evolution '*Q*' versus time. We have considered in this work that the architecture works in the same way as the memory

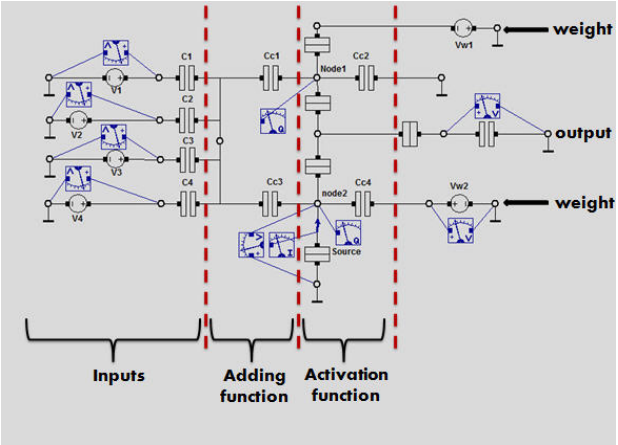

FIG.11 ELECTRICAL MODEL OF THE PROPOSED SET-BASED NEURAL CIRCUITRY 3-ISLAND BASED USING SIMON SIMULATOR

proposed in. In fact electrons are memorized in two islands and it depends on the inputs signal and the drain voltage which present the weight of the neuron**.** In order to better understand the operating mode of the architecture we should know that the various coupling capacitances between device elements, such as the capacitance of tunnel junction, C_{c1}, C_{c2}, C_{c3} and C_{c4} are extracted from SIMON simulator after several trials using stationary simulation. In fact, for every such time step 'even number' tunnel events are simulated and averaged.

In this part, we determine the shape of the charge *Q(t)* in the island which allows us to count the number of electrons stored in the memory nodes (node1 and node2) and to know the instant '*t*' when writing or erasing.

The simulation results using Simon software are shown in the Fig.12.

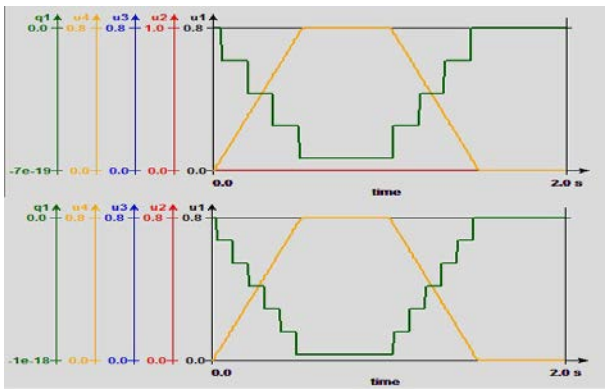

FIG.12.SIMULATION RESULTS WHEN THE NUMBER OF ELECTRONS INCREASES AS THE INPUTS INCREASE

Fig. 12 presents the SIMON simulation results in node 1 for different inputs and biased drain (weight) V_{ds}=V_{w1}=1mV. These results show that the number of electrons in the memory node (the green curve) after the charging increases when the input voltages increase until it reaches 6 electrons. Since energy levels are discrete, each state of charge or energy level is associated with an addition of an electron. All junction voltages have to be less than the critical voltage in order to hold the electron in the node. However, if inputs increase, the memory node can receive more electrons.

When V_{ins}=0.8V, there are electrons written in the memory node but after returning V_{ins} to zero electrons are lost.

The weights play the role of parameters which are adjusted at the training process. As we can see in Fig.13

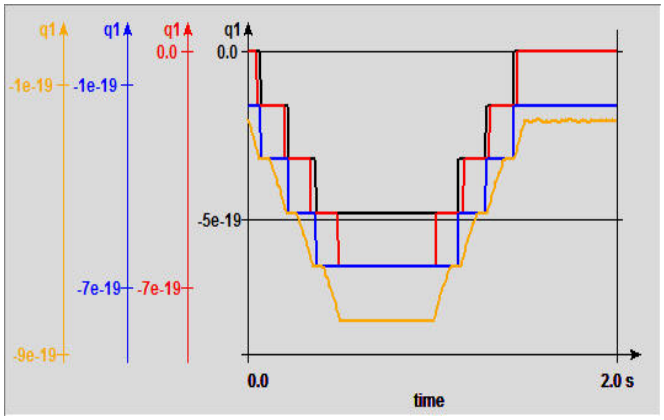

FIG.13.SIMULATION RESULTS OF THE CHARGE AND INFLUENCE OF WEIGHTS

We calculate the weight corresponding to the best functionality of the memory. The adequate weight, giving the charge-staircase curve (red curve), V_{w1} corresponding to the best memorization is -15.8 mV and has an influence on the shape of $q_1(t)$ and even the number of electrons written in the memory node. When the weight V_{w1} is equal to 2 mV three electrons are stored in the node1. By applying V_{w1} equal to 50 mV and more the memory lose the functionality.

As it is shown in Fig.14 when we increase the value of the capacitor from 1.5aF (black curve) to 15aF (red curve) and even V_{ins} returns to zero there still are charges in the node. This is because the thickness of the insulator of the capacitor is reduced and the electrons can pass from the mass to the node.

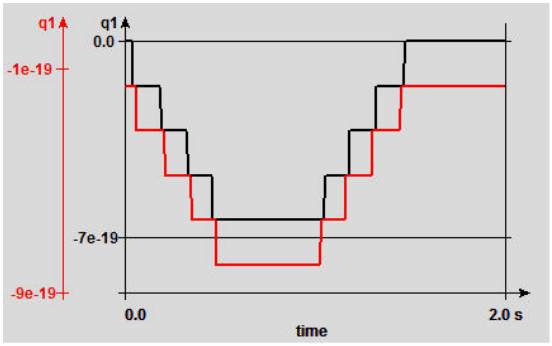

FIG.14.SIMULATION RESULTS OF THE CHARGE WHEN THE CAPACITOR C_{C2} INCREASE

Conclusion

In this paper a model for SET devices has been reported, MATLAB simulations are then successfully performed for different parameters. The model is able to describe the I_{ds} -V_{gs} and I_{ds}–V_{ds} characteristics. Besides, we have explained the principal of the operation of a single electron memory using a design of a 3-island based neuron circuit which has been presented and simulated by the SIMON tool.

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